

Arasan Chip Systems Announces Mixed Signal USB 2.0 PHY IP

Arasan acquires Mentor Graphics' silicon-proven USB 2.0 PHY

San Jose, California – October 18, 2011 –Arasan Chip Systems, Inc. (“Arasan”), the leading provider of Total IP Solutions for mobile storage and connectivity applications, announced today the availability of its USB 2.0 PHY IP. The USB 2.0 PHY comprises a complete on-chip physical transceiver solution optimized for low power consumption, minimal die area, and high data throughput. The USB2.0 PHY features fully integrated Electrostatic Discharge (ESD) protection, full support for OTG, device, hub and host functionality.

The core was developed by Mentor Graphics Corporation and proven in silicon in the SMIC 130nm process. Arasan has licensed the complete core and associated technology from Mentor Graphics and Arasan will support and develop the technology using its own analog mixed signal design team. “Acquiring this high-quality silicon-proven PHY core that successfully passed the USB plug-fest process has saved us a tremendous amount of development time.” said Prakash Kamath, Vice President of Engineering for Arasan. “Demand for USB 2.0 products continues to be robust.”

“For reasons unrelated to the USB market, we decided that the USB PHY business was not consistent with Mentor’s overall strategy. We are pleased to have Arasan carrying this technology and our investment legacy forward.” Said Aaik van der Poel, Business Unit Manager, Continuing Products Division, Mentor Graphics. “During the development effort we carefully constructed this IP to be compatible with standard CMOS processes for ease of porting and qualified it through the USB-IF plug fest methodology.”

The Arasan USB 2.0 PHY IP core is a high speed USB transceiver for use with host, embedded host, On-the-Go (OTG) and function controllers. Compliant with the USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) level 3 specification, the Arasan USB 2.0 PHY integrates high speed mixed-signal circuits to support USB High-Speed (HS) traffic at 480Mbps and is backward-compatible with 12Mbps Full-Speed (FS) and 1.5Mbps Low-Speed (LS) data rates.

The USB 2.0 PHY IP is delivered in a GDSII format targeted for a specific process technology library. Because the design was done with standard CMOS process technology in mind it can easily be ported to many foundry/process technology combinations.

The USB 2.0 PHY joins the suite of other Arasan USB products including USB 2.0 Device, Hub, OTG, embedded Host, HSIC PHY and USB 3.0 Device. Arasan's USB products benefit from:

Arasan's deep domain expertise – Arasan has been providing USB solutions ever since its founding 15 years ago and is an active member of the USB Implementers Forum (USB-IF). Arasan's engineering staff has extensive USB digital and analog backgrounds with up to 16 years of hands experience.

Proven IP quality that reduces risk – Arasan's USB IP has been used in production proven applications.

A comprehensive solution that reduces time to integration – Offered as a Total pre-certified IP solution including USB PHY 2.0 in addition to USB 2.0 Device, Hub and OTG Controller IP, Arasan also offers associated USB software stacks.

Knowledgeable support personnel to eliminate delays – Arasan's development engineering team provides direct support to customers insuring that the highest level of knowledge is immediately available to the customer thus reducing problem resolution time.

Availability

The Arasan USB 2.0 PHY IP solution, including IP core, verification IP and documentation is available immediately for licensing. Contact sales for availability on specific process technologies.

About Arasan

Arasan Chip Systems is a leading provider of Total IP Solutions for mobile storage and connectivity applications. Arasan's high-quality, silicon-proven, Total IP Solutions include digital IP cores, mixed signal and analog PHY interfaces, verification IP, hardware verification kits, protocol analyzers, software stacks and drivers and optional customization services for MIPI, USB, SD, SDIO, MMC/eMMC, CF, UFS, xD and many other popular standards. Arasan's Total IP products serve system architects and chip design teams in mobile, gaming and desktop computing systems that require silicon-proven, validated IP, delivered with the ability to integrate and verify both digital, analog and software components in the shortest possible time with the lowest risk.

Unlike many other IP providers, Arasan's Total IP Solution encompasses all aspects of IP development and integration, including analog and digital cores, hardware development kits, protocol analyzers, validation IP and software stacks and drivers and optional architecture consulting and customization services. Based in San Jose, CA, USA, Arasan Chip Systems has a 15 year track record of IP and IP standards development leadership.

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